TGA2578-CP

2 to 6 GHz, 30W GaN Power Amplifier

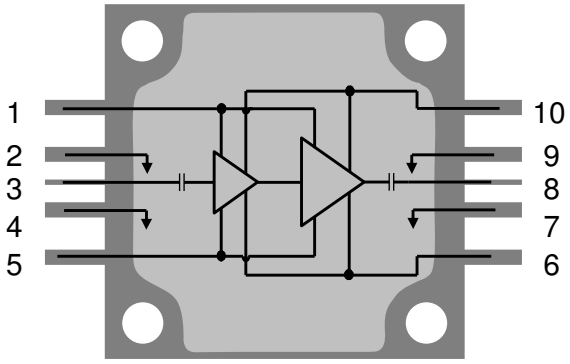
Applications

- Electronic Warfare
- Radar
- Communications
- Test Instrumentation
- EMC Amplifier

Product Features

- Frequency Range: 2 – 6 GHz
- Pout: 45 dBm at P_{IN} = 23 dBm
- PAE: >30% CW
- Small Signal Gain: >26 dB
- IM3: -30 dBc @ 30 dBm Pout/Tone
- Bias: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical
- Package Dimensions: 15.2 x 15.2 x 3.5 mm
- Package base is pure Cu offering superior thermal management

Functional Block Diagram



General Description

Qorvo's TGA2578-CP is a packaged wideband power amplifier fabricated on Qorvo's TQGaN25 0.25um GaN on SiC process. Operating from 2 to 6 GHz, the TGA2578-CP achieves 30 W saturated output power with a power-added efficiency of > 30 %, and > 26 dB small signal gain.

The TGA2578-CP is offered in a 10-lead 15 x 15 mm bolt-down package. The package has a pure Cu base, offering superior thermal management. The TGA2578-CP is ideally suited to support both commercial and defense applications.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 Ohms.

Lead free and RoHS compliant.

Evaluation Boards are available upon request.

Pin Configuration

Pad No.	Symbol
1, 5	V_G
2, 4, 7, 9	GND
3	RF_{IN}
6, 10	V_D
8	RF_{OUT}

Ordering Information

Part	ECCN	Description
TGA2578-CP	3A001.b.2.a	2 – 6 GHz, 30 W GaN Power Amplifier

Absolute Maximum Ratings

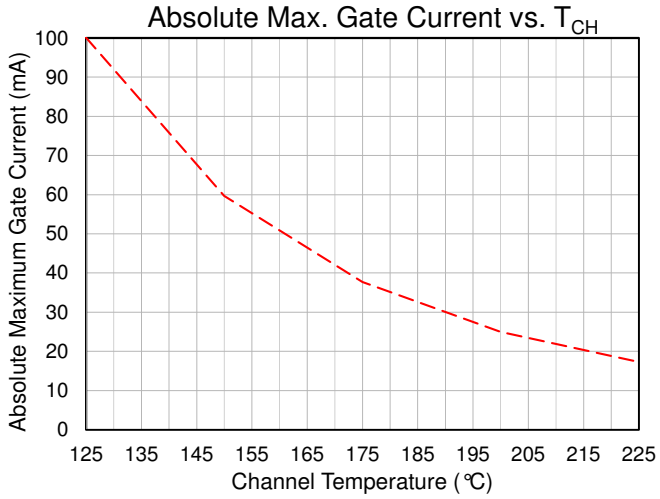
Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_D)	5 A
Reverse Gate Current (I_G)	-15 mA
Forward Gate Current (I_G)	See graph this page
Power Dissipation (P_{DISS}), 85℃	85 W
Input Power, CW, 50 Ω, (P_{IN})	27 dBm
Input Power, CW, VSWR 3:1, V_D = 30 V, 85 ℃, (P_{IN})	27 dBm
Input Power, CW, VSWR 10:1, V_D = 28 V, 85 ℃ (P_{IN})	25 dBm
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 Seconds)	260 ℃
Storage Temperature	-55 to 150 ℃

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	28 V
Drain Current (I_{DQ})	400 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 7
Gate Voltage (V_G)	–2.8 V (Typ.)
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 7
Temperature (T_{BASE})	-40 to 85 ℃

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.



Electrical Specifications

Test conditions unless otherwise noted: 25 ℃, V_D = 28 V, I_{DQ} = 400 mA, V_G = –2.8 V Typ, CW.

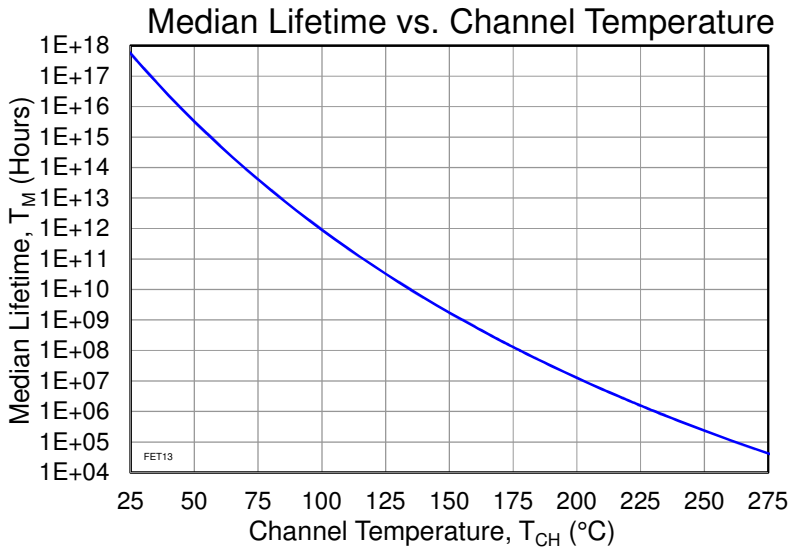
Parameter	Min	Typical	Max	Units
Operational Frequency Range	2.0		6.0	GHz
Small Signal Gain		> 26		dB
Input Return Loss		> 12		dB
Output Return Loss		> 5		dB
Output Power @ Pin = 23 dBm		45		dBm
Power Added Efficiency @ Pin = 23 dBm		> 30		%
IM3 (Pout/tone = 30 dBm/Tone)		-30		dBc
IM5 (Pout/tone = 30 dBm/Tone)		-40		dBc
Small Signal Gain Temperature Coefficient		-0.05		dB/℃
Output Power Temperature Coefficient		-0.02		dBm/℃

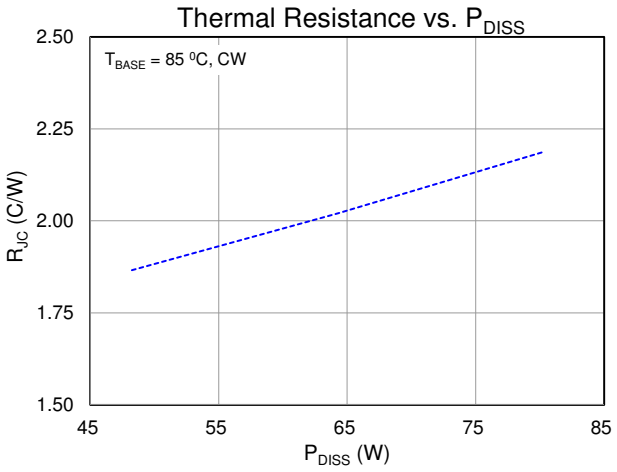
Thermal and Reliability Information

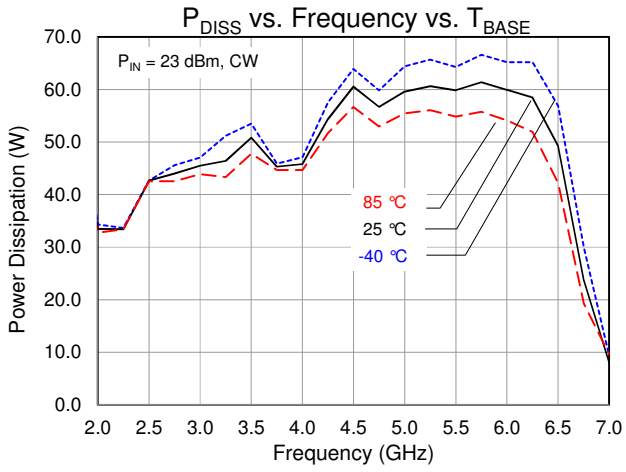
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 28 V (CW) At Freq = 5 GHz, P_{IN} = 23 dBm: I_{DQ} = 400 mA, I_{D_Drive} = 3.0 A P_{OUT} = 44 dBm, P_{DISS} = 55 W	1.95	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		192	°C
Median Lifetime (T_M)		2.6E+7	Hrs

Notes:
1. Thermal resistance measured to back of package.

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}



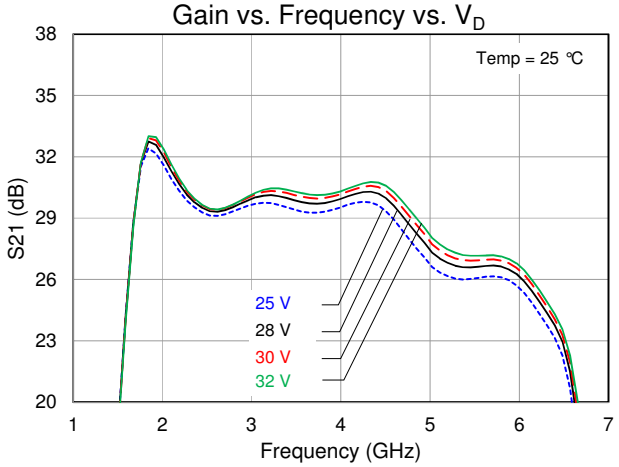




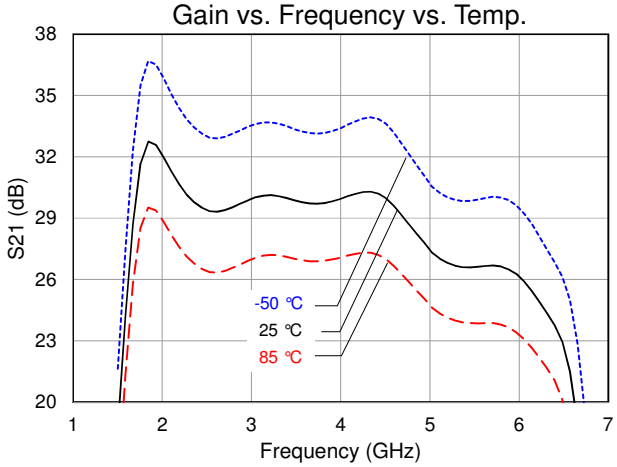
Typical Performance: Small Signal

Conditions unless otherwise specified: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical, CW.

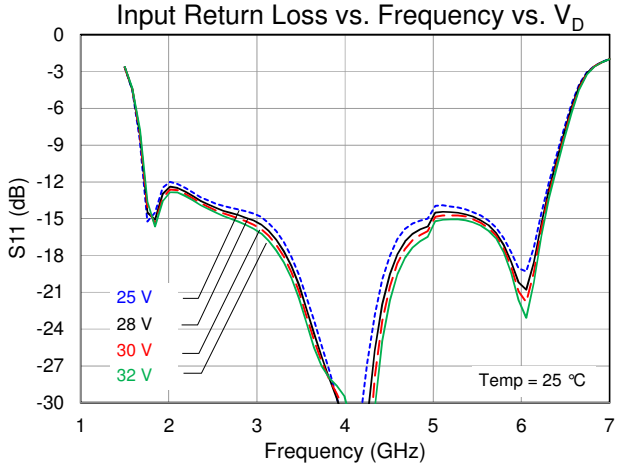
Gain vs. Frequency vs. V_D



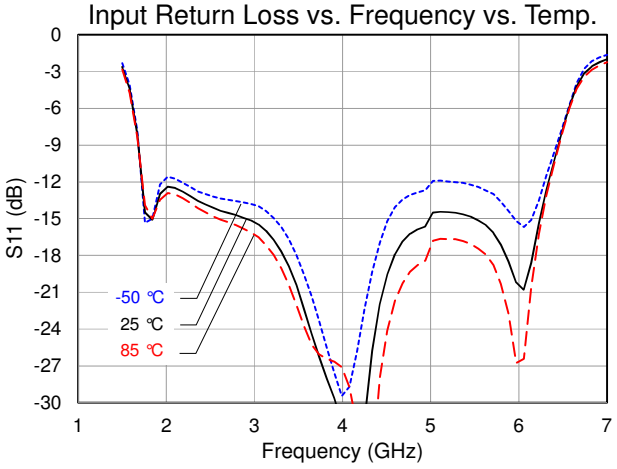
Gain vs. Frequency vs. Temp.



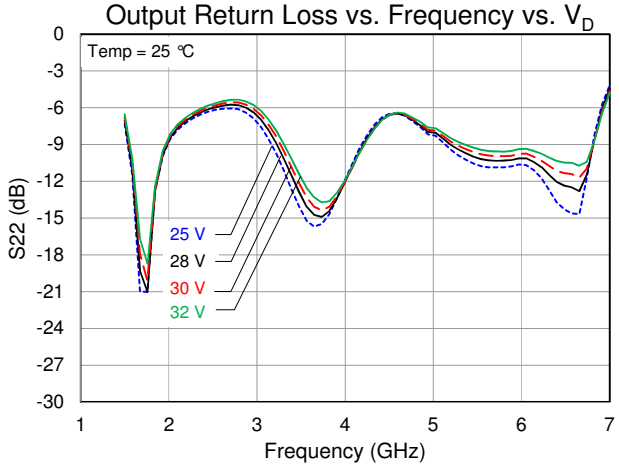
Input Return Loss vs. Frequency vs. V_D



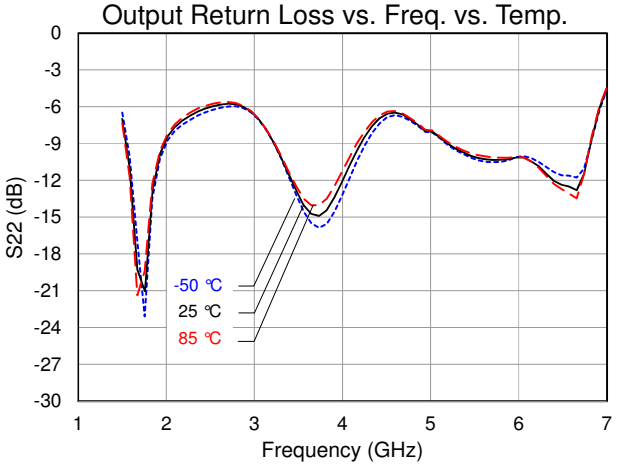
Input Return Loss vs. Frequency vs. Temp.



Output Return Loss vs. Frequency vs. V_D



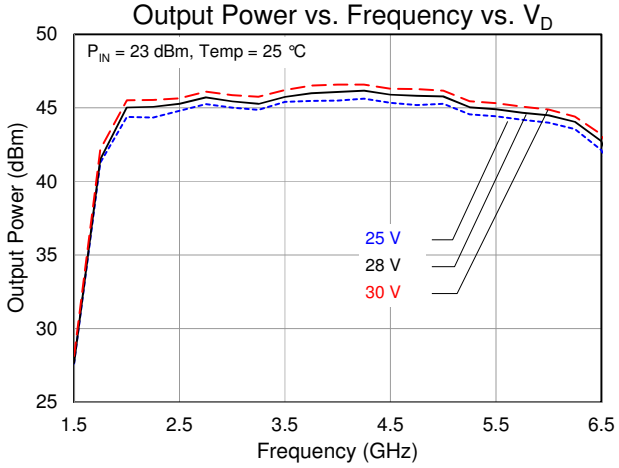
Output Return Loss vs. Freq. vs. Temp.



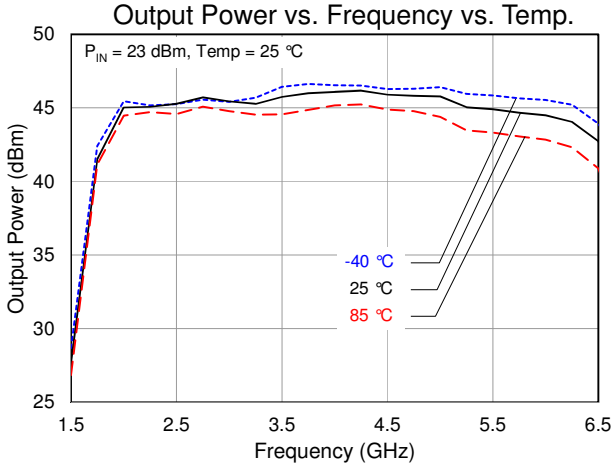
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical, CW.

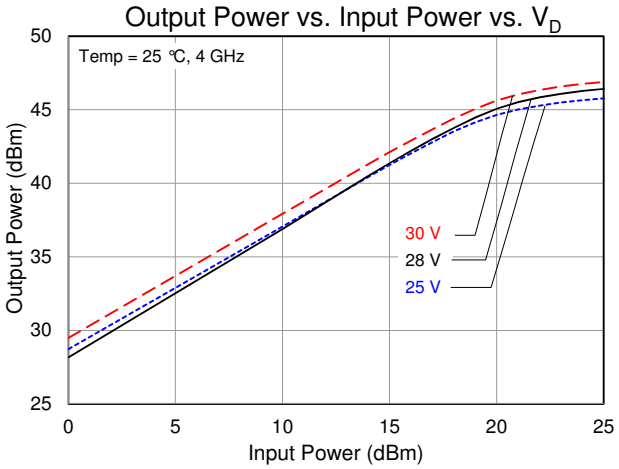
Output Power vs. Frequency vs. V_D



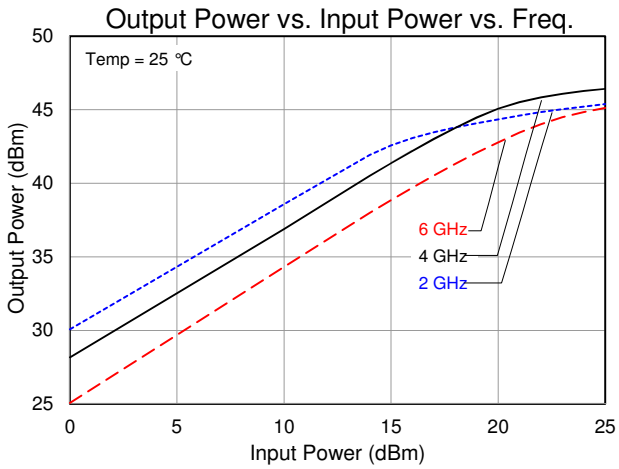
Output Power vs. Frequency vs. Temp.



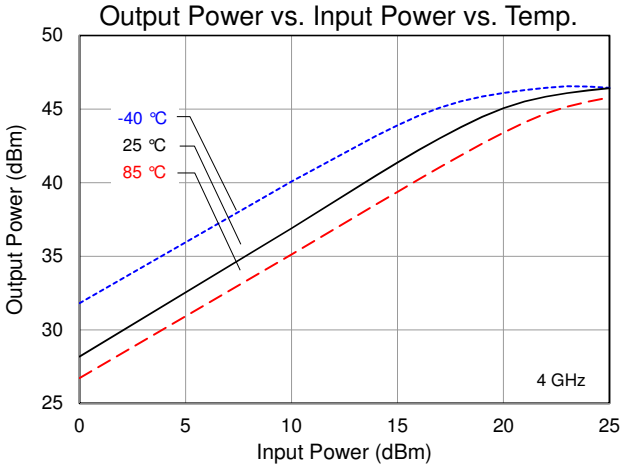
Output Power vs. Input Power vs. V_D



Output Power vs. Input Power vs. Freq.



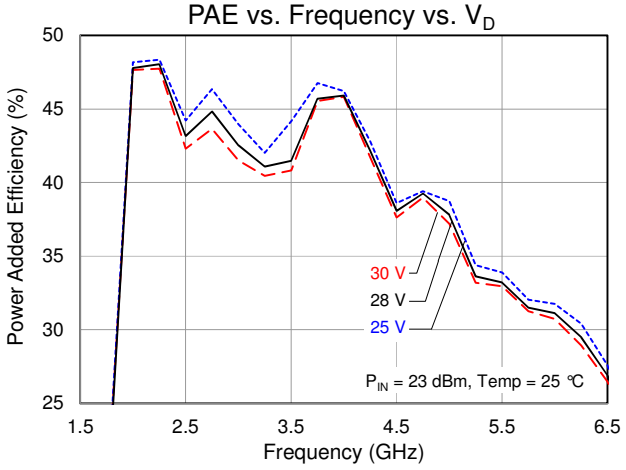
Output Power vs. Input Power vs. Temp.



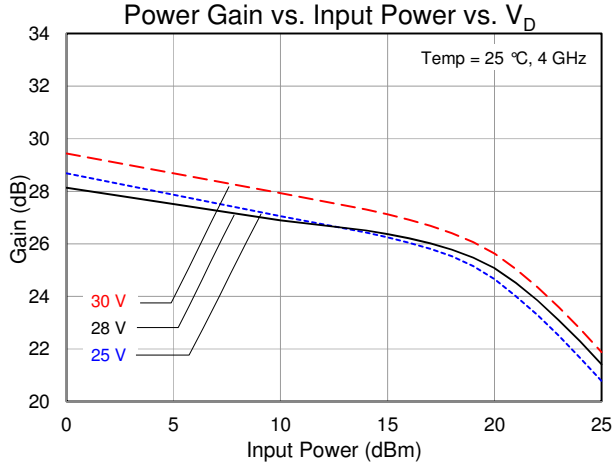
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical, CW.

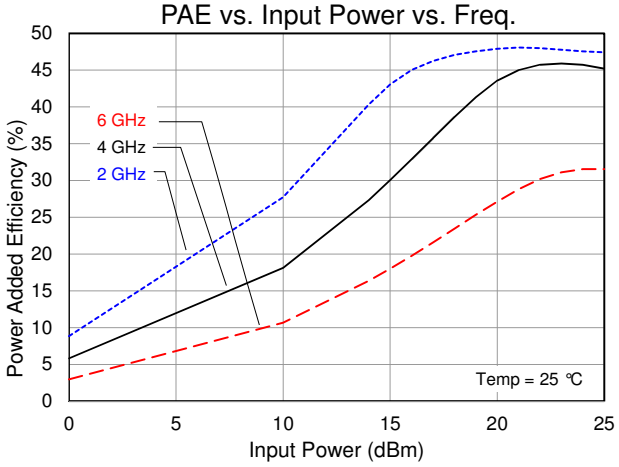
PAE vs. Frequency vs. V_D



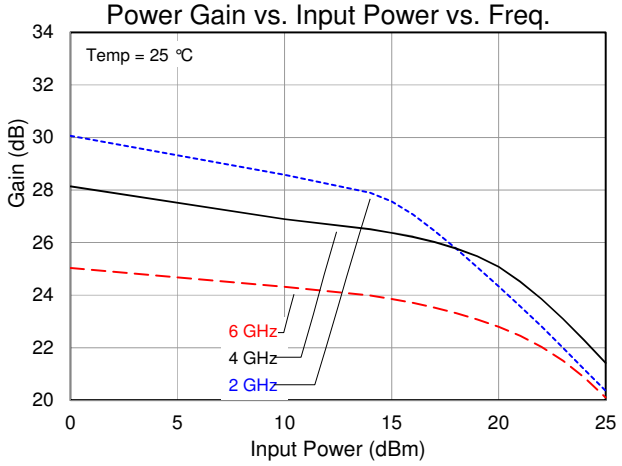
Power Gain vs. Input Power vs. V_D



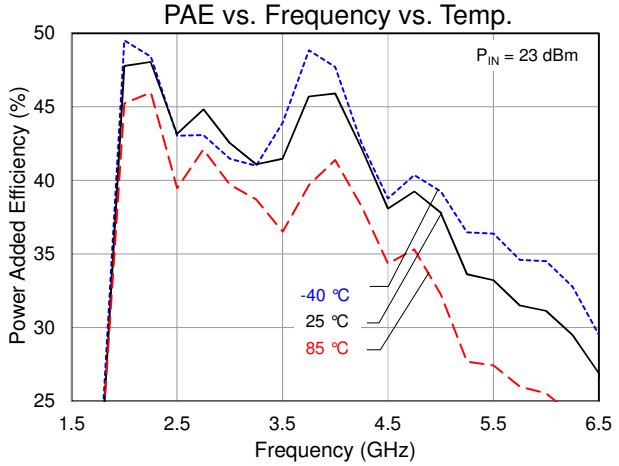
PAE vs. Input Power vs. Freq.



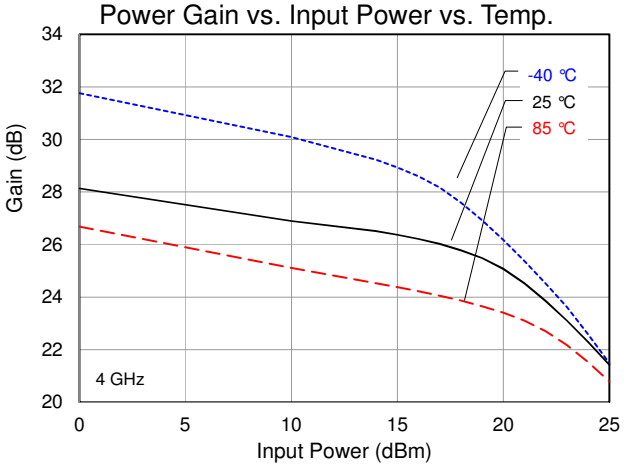
Power Gain vs. Input Power vs. Freq.



PAE vs. Frequency vs. Temp.



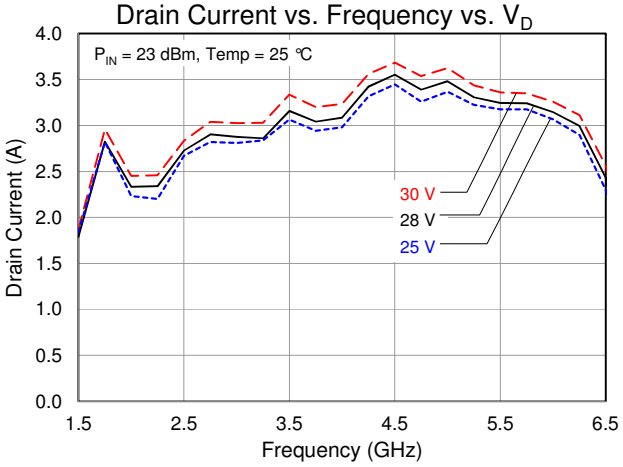
Power Gain vs. Input Power vs. Temp.



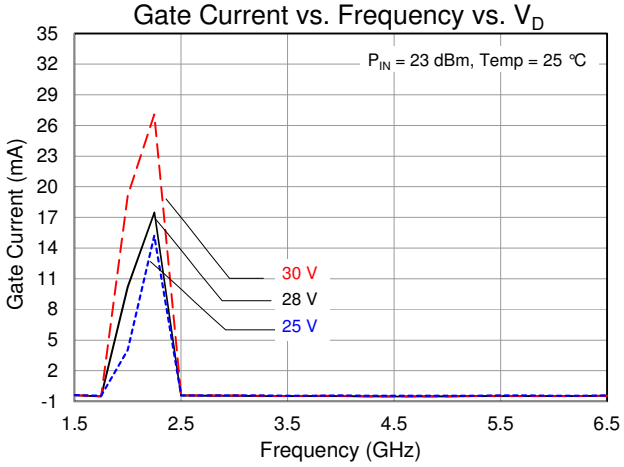
Typical Performance: Large Signal

Conditions unless otherwise specified: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical, CW.

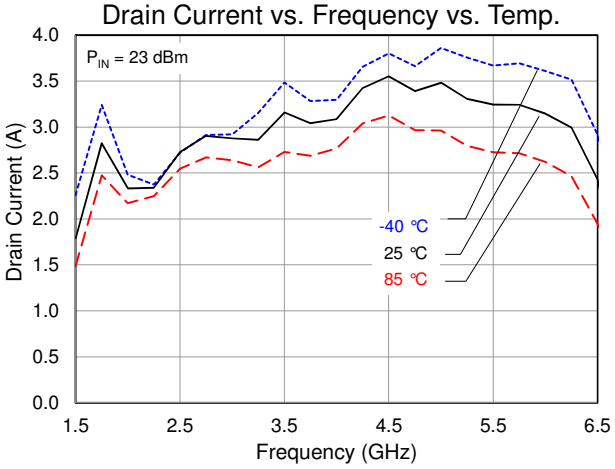
Drain Current vs. Frequency vs. V_D



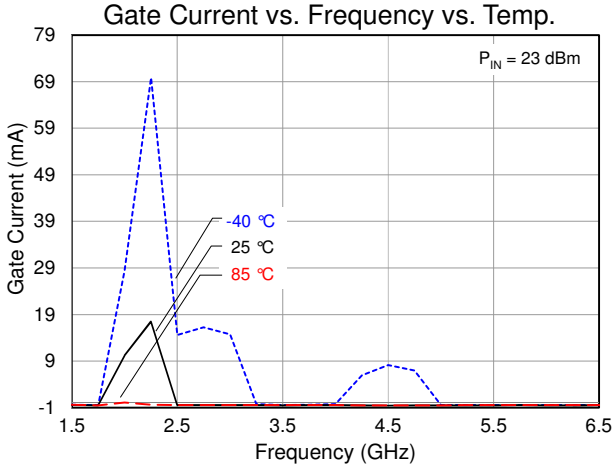
Gate Current vs. Frequency vs. V_D



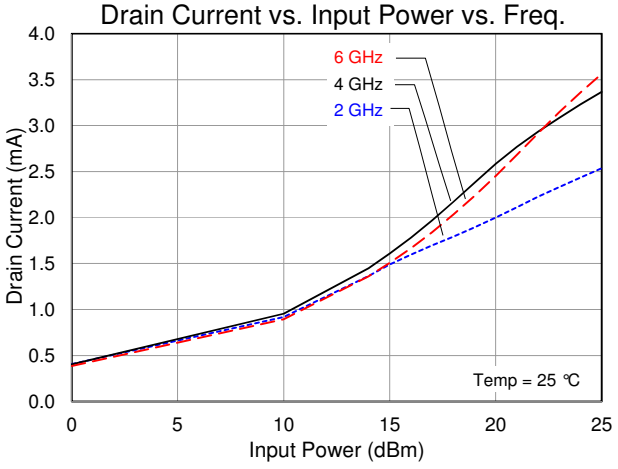
Drain Current vs. Frequency vs. Temp.



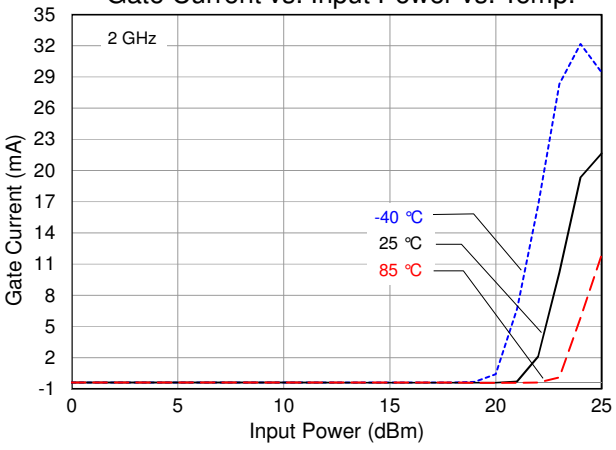
Gate Current vs. Frequency vs. Temp.



Drain Current vs. Input Power vs. Freq.



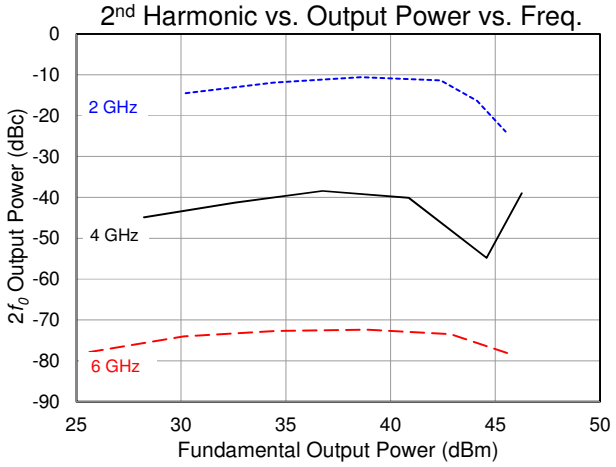
Gate Current vs. Input Power vs. Temp.



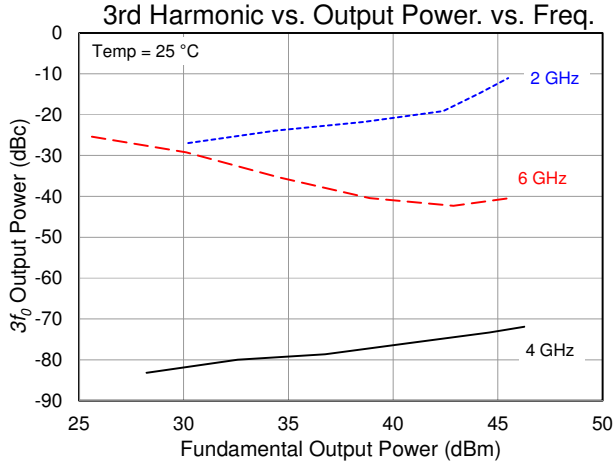
Typical Performance: Large Signal and Linearity

Conditions unless otherwise specified: V_D = 28 V, I_{DQ} = 400 mA, V_G = -2.8 V Typical, CW.

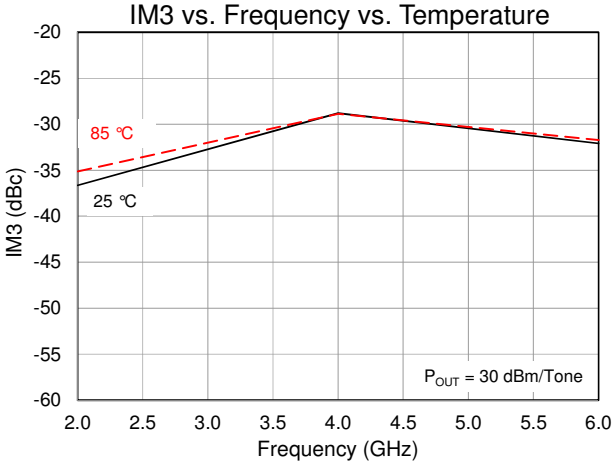
2nd Harmonic vs. Output Power vs. Freq.



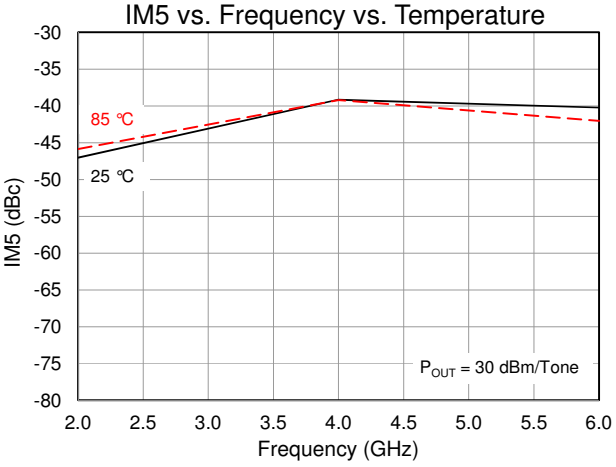
3rd Harmonic vs. Output Power. vs. Freq.



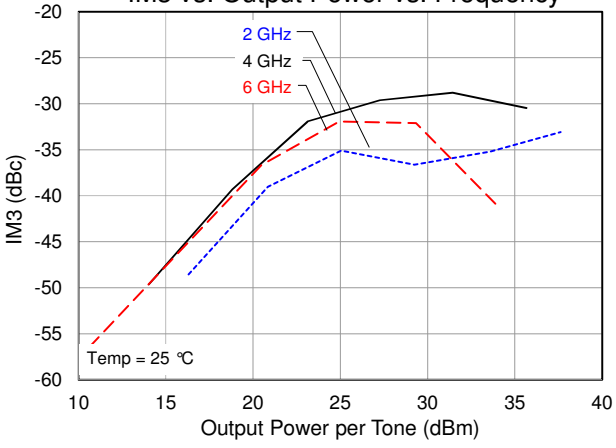
IM3 vs. Frequency vs. Temperature



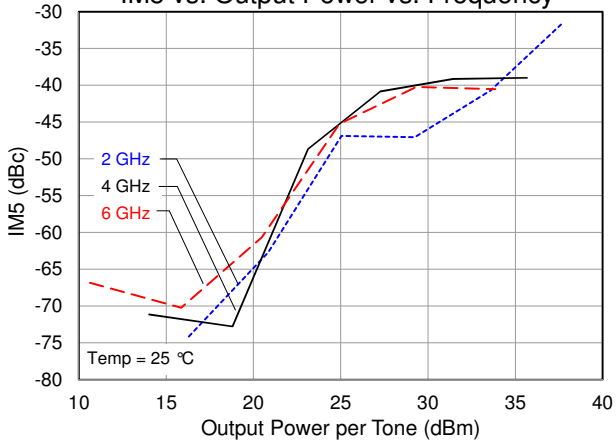
IM5 vs. Frequency vs. Temperature



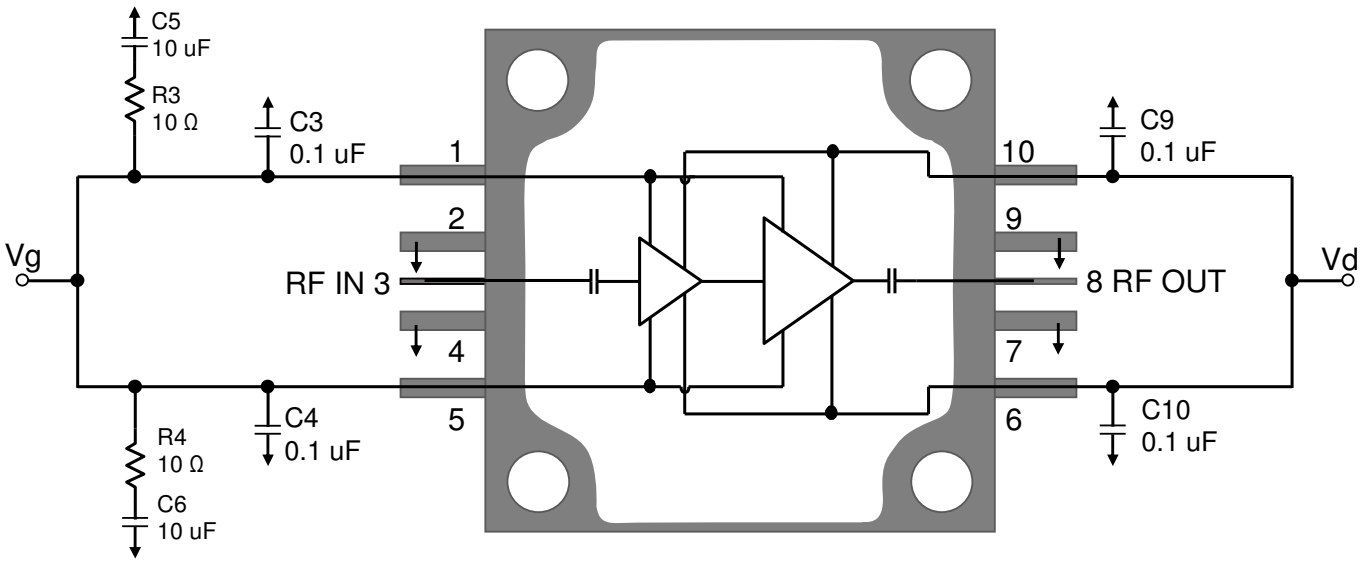
IM3 vs. Output Power vs. Frequency



IM5 vs. Output Power vs. Frequency



Applications Information and Pin Layout



Bias-up Procedure

1. Set I_D limit to 5 A, I_G limit to 25 mA
2. Apply –5 V to V_G
3. Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 400 mA (V_G ~ –2.8 V Typ.).
5. Turn on RF supply

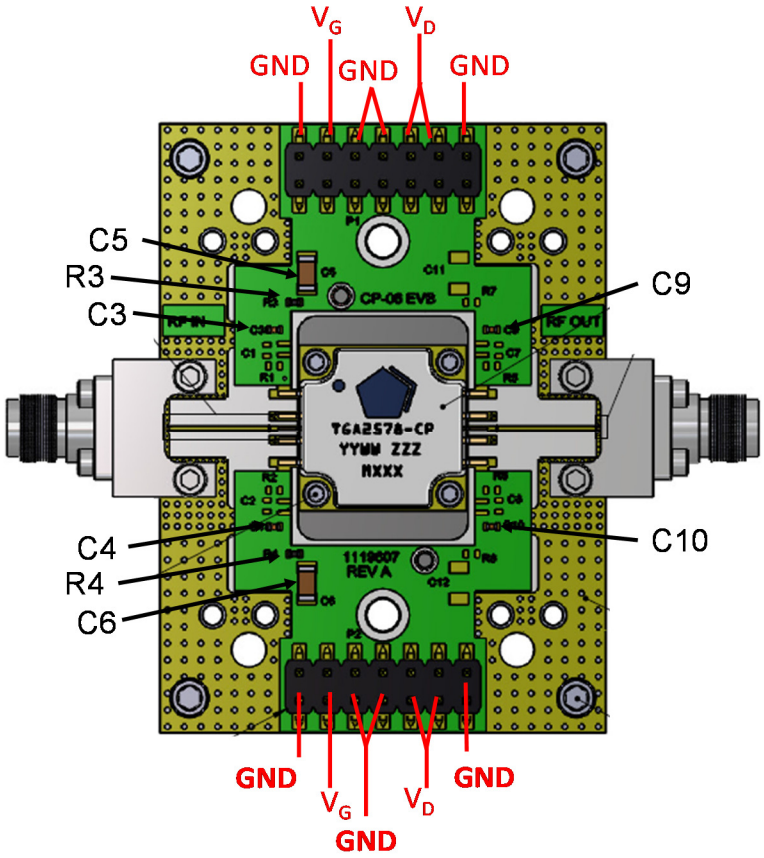
Bias-down Procedure

1. Turn off RF supply
2. Reduce V_G to –5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Pin Description

Pin No.	Symbol	Description
1,5	V_G	Gate Voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
3	RF_{IN}	Output; matched to 50 Ω; DC blocked
2,4,7,9	GND	Must be grounded on the PCB.
6,10	V_D	Drain voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
8	RF_{OUT}	Input; matched to 50 Ω; DC blocked

Evaluation Board



NOTE: Both Top and Bottom Vd and Vg must be biased.

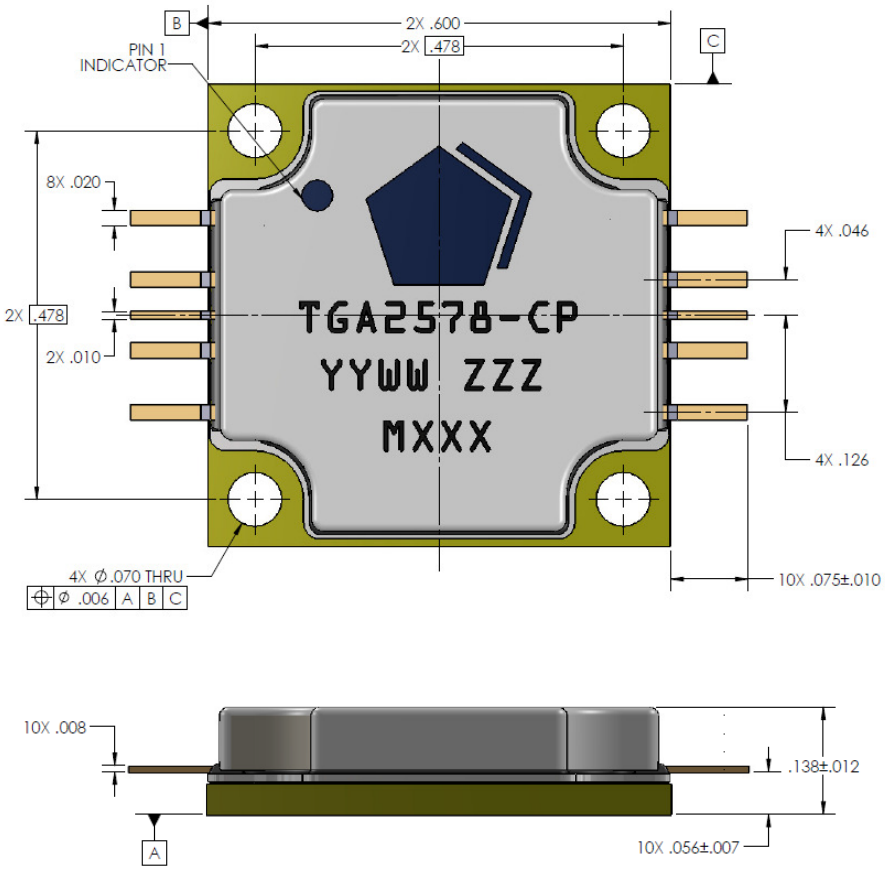
Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
C3, C4, C9, C10	0.1 µF	Cap, 0402, 50 V, 10%, X7R	Various	
C5, C6	10 µF	Cap, 1206, 50 V, 20%, X5R	Various	
R3, R4	10 Ohm	Res, 0402, 5%	Various	

Assembly Notes

1. Clean the board or module with alcohol. Allow it to dry fully.
2. Nylock screws are recommended for mounting the TGA2578-CP to the board.
3. To improve the thermal and RF performance, we recommend the following:
   a. Apply thermal compound or 4 mils indium shim between the package and the board.
   b. Attach a heat sink to the bottom of the board and apply thermal compound or 4 mils indium shim between the heat sink and the board.
4. Apply solder to each pin of the TGA2578-CP.
5. Clean the assembly with alcohol.

Mechanical Information



Units: inches
Tolerances: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
Materials:
Base: Copper
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2578: Part number
YY: Part Assembly year
WW: Part Assembly week
ZZZ: Serial Number
MXXX: Batch ID

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 0B
Value: 200 V
Test: Human Body Model (HBM)
Standard: JEDEC JS-001

MSL Rating

Level 5A at 260 °C convection reflow.
The part is rated Moisture Sensitivity Level 5A at 260 °C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce: 3A001.b.2.a

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260°C

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

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For technical questions and application information: **Email:** info-products@Qorvo.com

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